WHAT IS CLAIMED IS:

That Which Is Claimed Is:

1.A phase-changeable memory device comprising:

a substrate;

an insulating layer on the substrate, the insulating layer having a hole therein;

a first electrode in the hole in the insulating layer;

a pattern of a phase-changeable material on the first electrode; and

a second electrode on the layer of the phase-changeable material such that the pattern of the phase-changeable material is between the first and second electrodes, wherein portions of the second electrode extend beyond an edge of the pattern of phase-changeable material.

2.A phase-changeable memory device according to Claim 1 further comprising:

a second insulating layer on the second electrode and on the insulating layer, wherein the second electrode is between the second insulating layer and the pattern of phase-changeable material and wherein a void is defined between the portions of the second electrode extending beyond the edge of the pattern of the phase-changeable material and the first insulating layer.

3.A phase-changeable memory device according to Claim 2 wherein the second insulating layer comprises a material selected from at least one of silicon dioxide (SiO_2), silicon nitride (SiN_x), silicon oxide nitride (SiON), aluminum oxide (AlO_x), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), and/or hafnium oxide (HfO_2), and/or combinations thereof.

4.A phase-changeable memory device according to Claim 1 wherein a void is defined between the portions of the second electrode extending beyond the edge of the pattern of the phase-changeable material and the first insulating layer.

5.A phase-changeable memory device according to Claim 1 wherein the pattern of the phase-changeable material extends beyond the first electrode onto portions of the first insulating layer.

6.A phase-changeable memory device according to Claim 1 wherein the first insulating layer is free of the phase-changeable material.

7.A phase-changeable memory device according to Claim 1 wherein the phase-changeable material comprises a combination of at least one of tellurium (Te) and/or selenium (Se) and at least one of germanium (Ge), tin (Sb), bismuth (Bi), lead (Pb), tin (Sn), silver (Ag), sulphur (S), silicon (Si), phosphorus (P), oxygen (O), and/or nitrogen (N).

8.A phase-changeable memory device according to Claim 1 wherein each of the first and second electrodes comprises a conductive material including at least one of nitrogen, carbon, titanium, tungsten, molybdenum, tantalum, titanium silicide, tantalum, a silicide, and/or combinations thereof.

9.A phase-changeable memory device according to Claim 8 wherein each of the first and second electrodes comprises at least one of titanium nitride (TiN), tantalum nitride (TaN), molybdenum nitride (MoN), niobium nitride (NbN), titanium silicon nitride (TiSiN), titanium aluminum nitride (TiAlN), titanium boron nitride (TiBN), zirconium silicon nitride (ZrSiN), tungsten silicon nitride (WSiN), tungsten boron nitride (WBN), zirconium aluminum nitride (ZrAlN), molybdenum silicon nitride (MoSiN), molybdenum aluminum nitride (MoAlN), tantalum silicon nitride (TaSiN), tantalum aluminum nitride (TaAlN), titanium oxide nitride (TiON), titanium aluminum oxide nitride (TiAlON), tungsten oxide nitride (WON), and/or tantalum oxide nitride (TaON).

10.A phase-changeable memory device according to Claim 1 further comprising:

a protective insulating layer on sidewalls of the pattern of phase-changeable material, on exposed surfaces of the second insulating layer, and on the first insulating layer; and

a second insulating layer on protective insulating layer so that the protective insulating layer is between the second insulating layer and the second electrode and so that the protective insulating layer is between the second

insulating layer and the first insulating layer.

11.A phase-changeable memory device according to Claim 10 wherein a void is defined between the portions of the second electrode extending beyond the edge of the phase-changeable material and the first insulating layer.

12.A phase-changeable memory device according to Claim 10 wherein the protective insulating layer comprises a material selected from at least one of silicon dioxide (SiO_2), silicon nitride (SiN_x), silicon oxide nitride (SiON), aluminum oxide (AlO_x), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), and/or hafnium oxide (HfO_2), and/or a combination thereof.

13.A phase-changeable memory device according to Claim 1 further comprising:

a memory cell transistor included in the substrate, the memory cell transistor including spaced apart source/drain regions and a gate electrode therebetween, wherein the first electrode electrically coupled with one of the source/drain regions of the memory cell transistor.

14.A method of forming a phase-changeable memory device comprising:

forming an insulating layer on a substrate, the insulating layer having a hole therein;

forming a first electrode in the hole in the insulating layer;

forming a pattern of a phase-changeable material on the first electrode; and

forming a second electrode on the layer of the phase-changeable material such that the pattern of the phase-changeable material is between the first and second electrodes, wherein portions of the second electrode extend beyond an edge of the pattern of phase-changeable material.

15.A method according to Claim 14 wherein forming the pattern of phase-changeable material and forming the second electrode comprise,

forming a layer of the phase-changeable material on the first electrode and on the first insulating layer,

forming a layer of an electrode material on the layer of the phase-changeable material, and

after forming the layers of the phase-changeable material and the electrode material, patterning the layers of the phase-changeable material and the electrode material to provide the pattern of the phase-changeable material and the second electrode.

16.A method according to Claim 15 wherein the patterning the layers of the phase-changeable material comprises over etching the layer of the phase-changeable material with respect to the layer of the electrode material so that the portions of the second electrode extend beyond the edge of the pattern of phase-changeable material.

17.A method according to Claim 15 wherein patterning the layers of the phase-changeable material and the electrode material comprises forming an etch mask on the layer of the electrode material, etching portions of the layer of the electrode material exposed by the etch mask to provide the second electrode, etching the layer of the phase-changeable material using the etch mask and/or the second electrode as a mask, and removing the etch mask.

18.A method according to Claim 17 wherein etching portions of the layer of the electrode material comprises etching using an etch gas including CF_4, wherein etching the layer of the phase-changeable material comprises etching using an etch gas including CF_4 wherein a flux of the CF_4 decreases as etching the layer of the phase-changeable material progresses.

19.A method according to Claim 18 wherein the etch gasses for etching the layer of the electrode material and for etching the layer of the phase-changeable material include Ar and Cl_2.

20.A method according to Claim 17 wherein etching portions of the layer of the electrode material comprises etching using an etch gas including CF_4, Ar, and Cl_2, and wherein etching portions of the layer of the phase-changeable material comprises etching using an etch gas including Ar, and Cl_2 without CF_4.

21.A method according to Claim 14 further comprising:

forming a second insulating layer on the second electrode and on the insulating layer, wherein the second electrode is between the second insulating layer and the pattern of phase-changeable material and wherein a void is defined between the portions of the second electrode extending beyond the edge of the pattern of the phase-changeable material and the first insulating layer.

22.A method according to Claim 21 wherein the second insulating layer comprises a material selected from at least one of silicon dioxide (SiO_2), silicon nitride (SiN_x), silicon oxide nitride (SiON), aluminum oxide (AlO_x), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), and/or hafnium oxide (HfO_2), and/or combinations thereof.

23.A method according to Claim 14 wherein a void is defined between the portions of the second electrode extending beyond the edge of the pattern of the phase-changeable material and the first insulating layer.

24.A method according to Claim 14 wherein the pattern of the phase-changeable material extends beyond the first electrode onto portions of the first insulating layer.

25.A method according to Claim 14 wherein the first insulating layer is free of the pattern of phase-changeable material.

26.A method according to Claim 14 wherein the phase-changeable material comprises a combination including at least one of tellurium (Te) and/or selenium (Se) and at least one of germanium (Ge), tin (Sb), bismuth (Bi), lead (Pb), tin (Sn), silver (Ag), sulphur (S), silicon (Si), phosphorus (P), oxygen (O), and/or nitrogen (N).

27.A method according to Claim 14 wherein each of the first and second electrodes comprises a conductive material including at least one of nitrogen, carbon, titanium, tungsten, molybdenum, tantalum, titanium silicide, tantalum, a

silicide, and/or combinations thereof.

28.A method according to Claim 27 wherein each of the first and second electrodes comprises at least one of titanium nitride (TiN), tantalum nitride (TaN), molybdenum nitride (MoN), niobium nitride (NbN), titanium silicon nitride (TiSiN), titanium aluminum nitride (TiAlN), titanium boron nitride (TiBN), zirconium silicon nitride (ZrSiN), tungsten silicon nitride (WSiN), tungsten boron nitride (WBN), zirconium aluminum nitride (ZrAlN), molybdenum silicon nitride (MoSiN), molybdenum aluminum nitride (MoAlN), tantalum silicon nitride (TaSiN), tantalum aluminum nitride (TaAlN), titanium oxide nitride (TiON), titanium aluminum oxide nitride (TiAlON), tungsten oxide nitride (WON), and/or tantalum oxide nitride (TaON).

29.A method according to Claim 14 further comprising:

forming a protective insulating layer on sidewalls of the pattern of phase-changeable material, on exposed surfaces of the second insulating layer, and on the first insulating layer; and

forming a second insulating layer on the protective insulating layer so that the protective insulating layer is between the second insulating layer and the second electrode and so that the protective insulating layer is between the second insulating layer and the first insulating layer.

30.A method according to Claim 29 wherein forming the protective insulating layer comprises forming the protective insulating layer using at least one of atomic layer deposition and/or thermal chemical vapor deposition

31.A method according to Claim 29 wherein forming the second insulating layer comprises forming the second insulating layer using at least one of plasma vapor deposition and/or plasma enhanced chemical vapor deposition.

32.A method according to Claim 29 wherein a void is defined between the portions of the second electrode extending beyond the edge of the phase-changeable material and the first insulating layer.

33.A method according to Claim 29 wherein the protective insulating layer comprises a material selected from at least one of silicon dioxide (SiO_2), silicon nitride (SiN_x), silicon oxide nitride (SiON), aluminum oxide (AlO_x), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), and/or hafnium oxide (HfO_2), and/or a combination thereof.

34.A method according to Claim 14 further comprising:

forming a memory cell transistor in the substrate, the memory cell transistor including spaced apart source/drain regions and a gate electrode therebetween, wherein the first electrode is electrically coupled with one of the source/drain regions of the memory cell transistor.

35. A method of fabricating a phase-changeable memory device, the method comprising:

sequentially forming a phase-changeable material layer and an upper electrode layer on a substrate including a lower electrode;

etching the upper electrode layer using an etch gas including CF_4; and

etching the phase-changeable material layer, while decreasing CF_4 as the etching of the phase-changeable material progresses.

36. The method of claim 35, wherein the etch gas further includes Ar and Cl_2 gases.

37. A method of fabricating a phase-changeable memory device, comprising:

sequentially forming a phase-changeable material layer and an upper electrode layer on a substrate including a lower electrode;

etching the upper electrode layer using a mixture gas of Ar, Cl_2 and CF_4; and

etching the phase-changeable material layer, using a mixture gas of Ar and Cl_2.

38.A method according to Claim 37 wherein etching the phase-changeable material comprises etching the phase-changeable material layer without using CF_4.